

IN THE CLAIMS:

- Al
- 1 1. (Original) A method for processing a first memory request issued by a requestor and
2 directed to a location in a memory, the first memory request containing an address corre-
3 sponding to the memory location, the method comprising the steps of:
4 (A) associating the first memory request with a request identifier;
5 (B) selecting a memory device containing the memory location corresponding to
6 the address;
7 (C) issuing a second memory request without the request identifier to the memory
8 device to access information stored at the location;
9 (D) receiving the information from the memory device; and
10 (E) associating the information with the request identifier.
 - 1 2. (Original) The method of claim 1 wherein the first memory request further contains
2 the request identifier.
 - 1 3. (Original) The method of claim 1 wherein the step of associating the first memory
2 request with a request identifier further comprises the step of:
3 generating the request identifier.
 - 1 4. (Original) The method of claim 1 further comprising the steps of:
2 determining if the memory device is available; and
3 performing steps C through E if the memory device is available.
 - 1 5. (Original) The method of claim 1 further comprising the step of:
2 saving the address value and the request identifier.

- A1
- 1 6. (Original) The method of claim 1 wherein the requestor is a processor.
- 1 7. (Original) An apparatus for processing a first memory request issued by a requestor
2 and directed to a location in a memory, the first memory request containing an address
3 corresponding to the memory location, the apparatus comprising:
4 means for associating the first memory request with a request identifier;
5 means for selecting a memory device containing the memory location corre-
6 sponding to the address;
7 means for issuing a second memory request without the request identifier to the
8 memory device to access information stored at the location;
9 means for receiving the information from the memory device; and
10 means for associating the information with the request identifier.
- 1 8. (Original) The apparatus of claim 7 wherein the first memory request contains:
2 the request identifier.
- 1 9. (Original) The apparatus of claim 7 further comprising:
2 means for determining if the memory device is available.
- 1 10. (Original) The apparatus of claim 7 further comprising:
2 means for saving the request identifier.
- 1 11. (Original) The apparatus of claim 10 wherein the request identifier is saved in an en-
2 try in a table.
- 1 12. (Original) The apparatus of claim 7 wherein the first memory request contains
2 a port of origin.
- 1 13. (Original) The apparatus of claim 7 wherein the requestor is a processor.

1 14. (Original) A circuit for processing a first memory request issued by a requestor and
2 directed to a location in a memory, the memory comprising one or more memory devices,
3 the first memory request containing an address corresponding to the memory location, the
4 circuit comprising:

5 a system controller connected to the requestor and the memory, the system con-
6 troller configured to receive the first memory request from the requestor, associate the
7 first memory request with a request identifier and in response to the first memory request,
8 select one or more memory devices and issue one or more second memory requests with-
9 out the request identifier to each of the selected memory devices.

1 15. (Original) The apparatus of claim 14 wherein the system controller further com-
2 prises:

3 a table comprising one or more entries, each entry formatted with a request identi-
4 fier field and an address field, the request identifier field holding the request identifier
5 and the address field holding the address.

1 16. (Original) The circuit of claim 14 wherein the requestor is a processor.

1 17. (Original) An intermediate node configured to process a first memory request di-
2 rected to a location in a memory, the memory comprising one or more memory devices,
3 the first memory request containing an address corresponding to the memory location, the
4 intermediate node comprising:

5 a requestor configured to issue the first memory request;

6 a system controller coupled to the requestor, the system controller configured to
7 receive the first memory request, associate the first memory request with a request identi-
8 fier and in response to the first memory request select one or more memory devices and
9 issue one or more second memory requests without the request identifier to each of the
10 selected memory devices; and

A1
11 one or more memory devices coupled to the system controller, the memory de-
12 vices configured to receive the one or more second memory requests and return informa-
13 tion in response to the second memory requests.

1 18. (Original) The intermediate node of claim 17 wherein the system controller further
2 comprises:

3 a table comprising one or more entries, each entry formatted with a request identi-
4 fier field and an address field, the request identifier field holding the request identifier
5 and the address field holding the address.

1 19. (Original) The intermediate node of claim 17 wherein the requestor is a processor.

1 20. (Original) A computer readable medium comprising computer executable instruc-
2 tions for performing method recited in claims 1, 3, 4 or 5.

[Please add new claims 21 et seq. as follows:]

21. (New) Electromagnetic signals propagating on a computer network, comprising:

said electromagnetic signals carrying instructions for execution on a processor for
the practice of the method recited in claims 1, 3, 4 or 5.